REMARKS

Claims 1-5, 6-10 and 12-40 are pending. Claims 16-39 are withdrawn.

Applicants' Response to the Claim Rejections under 35 U.S.C. §103(a)

Claims 1, 2-4, 7, 9, 10, 12, 14 and 40 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (hereinafter, Chang) in view of Enomoto. In response thereto, applicants respectfully traverse on the basis that one of skill in the art would have no reason to modify the references so as to derive the currently claimed invention, and further, such a combination would not result in the claimed invention. Specifically, according to the present invention, as set forth in the parent claims the device region is free of a bird's beak structure.

Page 4 of the Office Action, cites to the descriptions of col. 1, lines 38-42 and col. 4, lines 28-37 of Enomoto as the reason for using "the gate insulating film having an uniform thickness at the region under the entire gate electrode teaching of Enomoto with Chang's device." Under U.S. patent law the prior art must be considered in its entirety, including disclosures that teach away from the claims. See MPEP 2141.02 VI[1]. Further, the Office must properly ascertaining the differences between prior art and claimed invention as provided by MPEP 2141.02.[2]

In regard to the entire teachings of Enomoto, the description of a manufacturing method of a semiconductor device as relied upon by the Office is found at column 4, line 52 to column

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1 A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)

[2] Ascertaining the differences between the prior art and the claims at issue requires interpreting the claims language,

5, line 33, and FIGS. 5-9. Therein, the first relevant step, as set forth in FIG. 5 requires the formation of an n-well 2 and a LOCOS oxide film 3. Next, in the process depicted at FIG. 6, a tunnel gate oxide film 5 and a floating gate layer 6 are formed. Thereafter, by thermal oxidation, an insulating film 7 is formed on the floating gate layer 6, and a gate oxide film 8 is formed on the surface of a field 4. As illustrated by FIG. 7, after formation of a polysilicon film 9, a memory cell is formed by selective etching, and ion implantation is performed for the source and drain regions of the memory cell. Thereafter, as exemplified in FIG. 8, patterning is performed for the gate of a peripheral transistor, and ion implantation is performed for the source and drain of an N-type transistor. Finally, in the process depicted in FIG. 9, ion implantation is performed for the source and drain of a P-type transistor. Wherefore, according to this manufacturing process of Enomoto, a bird's beak structure is formed in neither the peripheral portion nor the memory cell portion. That is, each of the tunnel gate oxide film 5 and the gate oxide film 8 has a uniform thickness.

Contrary, in the present invention as described on page 23, lines 15-18 and in FIGS. 9A through 9I:

> "As shown circled in FIG. 10A, in the step of FIG. 9C, bird's beaks are formed under the floating gate electrode pattern 13A with the formation of the protection insulating film 18."

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and considering both the invention and the prior art references as a whole.

On the other hand, in the process of FIG. 7 of Enomoto detailed above, no protection insulating film is formed to cover the multilayer gate electrode structure (6, 7, 9) in the memory cell portion after formation of the polysilicon film 9.

As such, in the current instance, in order to achieve Enomoto's object of exhibiting better and more desirable characteristics such as reducing damage and contamination without incurring cost, the entire teaching of Enomoto must be considered. In the relevant teachings of Enomoto, a bird's beak structure is not formed in the memory cell portion. Contrary, Chang requires that "the bird's beak is formed at an interface of the tunnel insulating film GX1 and the floating gate electrode GC1" as the Office admits on Page 3 of the Office Action.

Further, even if Chang and Enomoto are combined, the claimed semiconductor integrated circuit devices of the present invention, where a bird's beak structure is formed in the memory cell region while no bird's beak structure is formed in the device region, cannot be formed because a bird's beak structure is formed in both EPROM and the peripheral transistors of Chang while according to this manufacturing process of Enomoto, a bird's beak structure is formed in neither the peripheral portion nor the memory cell portion. Hence, Chang and Enomoto teach away from each other, and one of skill in the art would have no reason to make the combination of references. For at least the reasons set forth above, applicants respectfully submit that claims 1, 2-4, 7, 9, 10, 12, 14 and 40 are not obvious in light of the teachings of Chang in combination with Enomoto.

Claims 1 and 9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Fastow et al. (hereinafter, Fastow). In response thereto, applicants respectfully traverse on the basis that one of skill in the art would not make the combination in the manner proposed by the Office, because doing so would destroy the intended function of the device according to the teachings of the references.

In regard to independent claims 1 and 9, the Office relies on the silicide film 112 of FIG. 3 of Ono as alleged disclosure of the "protection insulation film" of the present invention. Referring to FIG. 3 of Ono, the silicide film 112 is formed only on the top surface of the multilayer gate electrode structure 107, 109, 111, and is not formed on its sidewall faces. The Office maintains that this deficiency is cured by the thin layer of oxide 314 of Fastow. See page 9 of the Office Action.

According to the manufacturing method of Ono, a first polysilicon film 107 and a second polysilicon film and a second polysilicon film 111 are formed as gate electrodes. Thereafter, a silicide film 112 is formed on a memory cell and a peripheral transistor. Next, etching is performed to form the gate electrode of the memory cell. Then, etching is performed for the gate electrode of the peripheral transistor. Finally, an LDD structure is formed for the peripheral transistor and a source and drain are formed for the memory cell. See column 2, line 56 to column 3, line 62 and Figs. 1A-3.

Under U.S. patent law a proposed modification cannot change the principle of operation of a reference. See MPEP 2143.01 VI[3]. In the current instance, modifying Ono with the teaching (thin layer of oxide 314) of Fastow substantially changes the principle of operation of Ono. Specifically, the manufacturing process of Ono, in which the silicide film 112 is formed in the process of FIG. 1D, detailed above, is not obtainable, because it is extremely difficult or impossible to form the silicide film 112 so that the silicide film 112 also covers the sidewall faces of the multilayer gate electrode structure 107, 109, 111. Further, even if Ono is modified with the teaching of Fastow, employment of the teaching of Fastow results in formation of a bird's beak structure in each of the memory cell and the peripheral transistor. As such, one of skill in the art reviewing the references would not have a reason to modify Ono based on Fastow to obtain the currently claimed invention. Specifically, doing so is contrary to the manufacturing processes of Ono and Fastow. When interpreted as a whole the references teach a structure outside the scope of the claimed invention; namely, a bird's beak structure in both the memory cell and the peripheral transistor regions. Wherefore, claims 1 and 9 are not obvious in light of Ono in view of Fastow, because the modification to the process of Ono is destructive to that process, and Fastow does not provide a reason to modify Ono in a manner which is read on by the currently pending claims.

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[3] If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)

Claims 6 and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chang and Enomoto and further in view of Prall et al. Claims 8 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chang and Enomoto and further in view of Applicant Admitted Prior Art (APA). Applicants respectfully submit that by addressing parent claims 1 and 9, as detailed above, the rejections of claims 6, 8, 13 and 15 should likewise be considered addressed by nature of their dependency.

In view of the aforementioned remarks, Applicants submit that the claims as previously presented are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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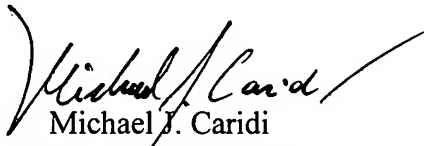

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